## REMARKS

Reexamination and reconsideration of this application in view of the following remarks is respectfully requested.

### Claim Rejections - 35 USC §103

Reconsideration of the rejection of claims 1-26 under 35 U.S.C. §103(a) as being unpatentable over Zolnowsky (U.S. 5,826,081) in view of Wah Chan et al., (U.S. 2002/0046334) hereinafter "Wah Chan", is respectfully requested for the following reasons.

Referring now to the rejection of claim 1, the Applicants agree with the Examiner that Zolnowsky does not explicitly disclose the first process executing writes using a compare and swap instruction.

The Applicants disagree with the Examiner's interpretation of Wah Chan. When an instruction may require writing to a memory location, Wah Chan teaches that the instruction is allowed to lock the memory location before determining whether the instruction is to be executed to completion. This "early locking" allows the instruction to begin operation earlier than with prior art methods, by allowing reading from the memory location prior to determining whether the instruction is to be completed. Using prior art methods, locking the memory location before determining whether the instruction is to be executed to completion is dangerous because the instruction may be canceled before completion, thereby permanently locking the memory location. Wah Chan overcomes this disadvantage of locking the memory location early by including within the instruction the step of always unlocking the memory location later in the instruction processing. Therefore, Wah Chan does not concern itself with prioritized and non-prioritized CPUs. The two CPUs of Wah Chan (CPU 120.1 and CPU 120.2) have equal priority.

The Examiner stated in the Office Action, "*However, Wah Chan teaches using the swap and compare instruction prior to the locking of the resource by any particular CPU as illustrated in Figure 1, page 1, paragraph 0019.*" The Applicants disagree with this statement by the Examiner. For convenience, paragraph 0019 is reproduced below.

> "[0019] Data cache 130 includes a set-associative cache memory 130M and control logic (not shown) to access the cache memory. Such caches are known in the art. Each cache set 130L in memory 130M can store a number of data words W0, W1 . . . (thirty-two 32-bit words in some embodiments). In addition, each cache set 130L includes a lock bit L which indicates whether the cache set is locked, and a processor bit P which indicates which CPU has locked the cache set. When the cache set is locked, the cache set can be accessed only from the port connected to the CPU that has locked the cache set. The other CPU is not allowed to read or write the cache set or those memory 140 locations whose contents are cached in the cache set."

As one can see by carefully re-reading paragraph 0019, Wah Chan does **not** explicitly disclose using the swap and compare instruction prior to the locking of the resource by any particular CPU. Nor does Figure 1 of Wah Chan explicitly disclose using the swap and compare instruction prior to the locking of the resource by any particular CPU. Nor does Wah Chan, as a whole, disclose using the swap and compare instruction prior to the locking of the resource by any particular CPU. Paragraph 0019 merely states that when a cache set has been locked by one of the CPUs, the cache set cannot be accessed by the other CPU.

The Examiner stated in the Office Action, "*Wah Chan teaches a prioritized information processing unit acquiring the contended resource by a second process to the exclusion of the non-prioritized information processing unit having acquired the non-prioritized exclusion right, the second process executing writes by using normal write instructions. When the CPU selected has locked the resource, the normal write sequence is used, page 2, paragraph 0034.*" The Applicants disagree with this statement by the Examiner. Wah Chan does not disclose that a normal write sequence is used when the selected CPU has locked the resource. For convenience, paragraph 0034 is reproduced below.

> "[0034] If the data requested at step 310 are in the cache, and the cache set has not been locked by CPU 120.2, the DCU returns the data on lines 170D. Otherwise, the DCU asserts appropriate controls signals (not shown) to CPU 120.1 to signal that the cache set is locked or the data are not in the cache, whatever the case may be. If the data are not in the cache, CPU 120.1 issues a request to bus interface unit (BIU) 180 to fetch the data from memory 140. BIU 180 fetches the data via bus 190. When the data are fetched, they are cached in a cache set 130L in DCU 130 and are also provided to CPU 120.1. In addition, the lock bit L is set in the cache set, and the processor bit P is made to indicate CPU 120.1."

As one can see by carefully re-reading paragraph 0034, Wah Chan does not disclose that a normal write sequence is used when the selected CPU has **locked** the resource. Paragraph 0034 merely describes how CPU 120.1 accesses the cache if the cache has **not been locked** by CPU 120.2. Paragraph 0034 also merely describes what happens when CPU 120.1 attempts to access the cache when the cache has been locked by the CPU 120.2, but such description does **not** include describing a normal write sequence.

Therefore, the combination of Zolnowsky and Wah Chan fails to disclose all the elements of claim 1. Accordingly, the Applicants believe that claim 1 should be allowed. Furthermore, claims 2-13, 17 and 21 depend upon independent claim 1, and because dependent claims recite all the limitations of the independent claim, it is believed, for this additional reason, that dependent claims 2-13, 17 and 21 also recite in allowable form.

The reasons set forth hereinabove with regard to claim 1 apply equally as well to independent claims 15 and 19; therefore, claims 15 and 19 should also be allowed. Furthermore, claims 22-24 depend upon independent claim 19, and because dependent claims recite all the limitations of the independent claim, it is believed, for this additional reason, that dependent claims 22-24 also recite in allowable form.

Accordingly, in view of the remarks above, and because combination of Zolnowsky and Wah Chan does not teach, anticipate or suggest, the presently claimed invention, the Applicants believe that the rejection of claims 1-26 under 35 U.S.C. §103(a) has been overcome. The Applicants request that the Examiner withdraw the rejection of these claims.

## Conclusion

The foregoing is submitted as full and complete response to the Office Action mailed January 4, 2007, and it is submitted that claims 1-26 are in condition for allowance. Reconsideration of the rejection is requested. Allowance of claims 1-26 is earnestly solicited.

No amendment made was related to the statutory requirements of patentability unless expressly stated herein. No amendment made was for the purpose of narrowing the scope of any claim, unless the Applicants have argued herein that such amendment was made to distinguish over a particular reference or combination of references.

The Applicants acknowledge the continuing duty of candor and good faith to disclose information known to be material to the examination of this application. In accordance with 37 CFR §1.56, all such information is dutifully made of record. The foreseeable equivalents of any territory surrendered by amendment are limited to the territory taught by the information of record. No other territory afforded by the doctrine of equivalents is knowingly surrendered and everything else is unforeseeable at the time of this amendment by the Applicants and their attorneys.

The present application, after entry of this response, comprises twenty-six (26) claims, including three (3) independent claims. The Applicants have previously paid for twenty-six (26) claims including six (6) independent claims. The Applicants, therefore, believe that a fee for claims amendment is currently not due.

**If the Examiner believes that there are any informalities that can be corrected by Examiner's amendment, or that in any way it would help expedite the prosecution of the patent application, a telephone call to the undersigned at (561) 989-9811 is respectfully solicited.**

The Commissioner is hereby authorized to charge any fees that may be required or credit any overpayment to Deposit Account **50-1556**.

In view of the preceding discussion, it is submitted that the claims are in condition for allowance. Reconsideration and re-examination is requested.

Respectfully submitted,

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